REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

After entry of the foregoing amendments, Claims 1-11 are pending in the present application. Claims 1-3, 5, 6, and 8-11 are amended by the present amendment. No new matter is added. As the amendments are not believed to require further search or consideration of the prior art, Applicant respectfully requests entry of the amendments.

In the outstanding Office Action, the specification was objected to under 35 U.S.C. 132(a); Claims 1-11 were rejected under 35 U.S.C. 112, first paragraph; Claims 1-4 and 8 were rejected under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,518,833 to Narendra et al. (hereinafter "Narendra"); Claims 1 and 5 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 6,771,117 to Nakai; and Claims 6, 7, and 9-11 were indicated as reciting allowable subject matter.

Applicants note, with appreciation, the indication of allowable subject matter.

Regarding the objection to Applicant's specification under 35 U.S.C. 132(a), Applicant respectfully submits the objection is improper because the amended language "from the exterior" was added only to the claims. The MPEP states:

> If new subject matter is added to the disclosure, whether it be in the abstract, the specification, or the drawings, the examiner should object to the introduction of new matter under 35 U.S.C. 132 or 251 as appropriate, and require applicant to cancel the new matter. If new matter is added to the claims, the examiner should reject the claims under 35 U.S.C. 112, first paragraph - written description requirement.[1]

Accordingly, Applicant respectfully requests that the objection to the specification under 35 U.S.C. 132(a) be withdrawn.

Addressing now the rejection of Claims 1-11 under 35 U.S.C. 112, first paragraph, that rejection is respectfully traversed.

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[1] MPEP § 2163.06.

The Office Action states that Applicant's specification does not support the added claim limitation "from the exterior" of the bias generating circuit; and further states, "There is nothing disclosed in the original specification establishing that this signal is in any [way] 'from the exterior.'"[2] However, an applicant is not required to show *verbatim* support for the added claim language. Rather, the MPEP states:

> What is conventional or well known to one of ordinary skill in the art need not be disclosed in detail. See *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d at 1384, 231 USPQ at 94. **If a skilled artisan would have understood the inventor to be in possession of the claimed invention** at the time of filing, **even if every nuance of the claims is not explicitly described** in the specification, then the adequate description requirement is met. See, e.g., *Vas-Cath*, 935 F.2d at 1563, 19 USPQ2d at 1116; *Martin v. Johnson*, 454 F.2d 746, 751, 172 USPQ 391, 395 (CCPA 1972) (stating "the description need not be in *ipsis verbis* [i.e., "in the same words"] to be sufficient").[3] (emphasis added).

In view of at least the first embodiment of the present application, Applicant is clearly in possession of the claimed voltage signal "input from the exterior of the bias voltage generating circuit". In that non-limiting embodiment, Figures 1 and 2 illustrate a differential amplifier circuit and a **separate** bias voltage generating circuit, respectively. In a feedback action, the bias voltage generating circuit outputs a bias voltage signal to the differential circuit in response to a reference voltage signal in the differential amplifier circuit.[4] Clearly, if the disclosed feedback action of the bias voltage generating circuit is responsive to a voltage signal in a separate circuit, then Applicant's disclosure supports the claimed input of a voltage signal "from the exterior" of the bias voltage generating circuit.

Accordingly, Applicant respectfully requests that the rejection of Claims 1-11 under 35 U.S.C. 112, first paragraph, be withdrawn. Alternatively, if the rejection is not withdrawn, Applicants respectfully request an explanation as to why a person skilled in the art would not

[2] Office Action 04/22/2005, page 2.
[3] MPEP § 2163.
[4] Specification, page 12, line 22 – page 13, line 2.

conclude the reference voltage signal is input from an exterior of the bias voltage generating circuit.[5]

Addressing now the rejection of Claims 1-4 and 8 under 35 U.S.C. 102(e) as anticipated by Narendra, that rejection is respectfully traversed.

"[W]hen evaluating the scope of a claim, every limitation in the claim must be considered. Office personnel may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, the claim as a whole must be considered."[6] The claimed recitation of "from the exterior" clarifies that the voltage signal is not limited to the bias voltage generating circuit. However, the "signal gate of [transistor] 124" (cited as teaching the claimed voltage signal) is limited to within Narendra's voltage reference circuit. Moreover, if the voltage at the gate of transistor 124 is input "from the exterior" of the current mirror circuits formed by Vcc, Vss, branches 102, 104, 106, and transistor 124, then those current mirror circuits would not function properly. In other words, as the voltage at the gate of transistor 124 must be input from within the above-noted current mirror circuits, that voltage cannot be input from the exterior of Narendra's voltage reference circuit.

Accordingly, for the above-stated reasons, Applicant respectfully requests that the rejection of Claims 1-4 and 8 under 35 U.S.C. 102(e) as anticipated by Narendra be withdrawn.

Addressing now the rejection of Claims 1 and 5 under 35 U.S.C. 103(a) as unpatentable over Nakai, that rejection is respectfully traversed.

Amended Claim 1 recites that "said first bias voltage varies in accord with changes in an absolute value of said voltage signal". In a non-limiting example, Applicant's Figures 1

[5] MPEP 2163.04 states, "The examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims." The conclusion that "there is nothing disclosed in the original specification establishing that this signal is in any way 'from the exterior'" does not appear to satisfy this burden.
[6] MPEP § 2106(II)(C).

and 2 illustrate how the claimed variation can ensure a constant current. As stated with respect to those figures:

> In this bias voltage generating circuit [of Figure 2], when an absolute value of the reference voltage signal Vref changes, a voltage between the gate and the source of the Pch MOS transistor M3 changes. According to this, a voltage drop amount between the drain and the source of the Pch MOS transistor M3 changes, and the bias voltage biasn can be made to change. ...
>
> Thus, in the differential amplifier circuit in FIG. 1, even if the common mode voltage of the reference voltage signal Vref decreases and the current flowing through the Nch MOS transistor NT3n decreases, the bias voltage biasn to the Nch MOS transistor NT3n rises and thus the current flowing through the Nch MOS transistor NT3n increases, and the bias voltage generating circuit in FIG. 2 has a feedback action ensuring a constant current value through the Nch MOS transistor NT3n which is a constant current circuit.[7]

The outstanding Office Action cites Nakai's Figure 2 as teaching the claimed invention. However, as the Office Action does not cite a component teaching the claimed first transistor, Applicants cannot discern the manner in which Nakai is asserted as teaching the claimed invention.

The Office Action cites both Nakai's transistor P11 and resistor R8 as teaching the claimed second transistor. Thus, Applicants presume that one of those components is asserted as teaching the claimed first transistor (which has a gate that receives the claimed voltage signal). As transistor N9 is cited as teaching the claimed first current generating part (which supplies a first potential to the claimed first transistor), Applicants presume the Office Action is asserting only Nakai's resistor R8 as teaching the claimed first transistor.

However, Claim 1 recites that "said first bias voltage varies in accord with changes in an absolute value of said voltage signal". Thus, the claimed first transistor inputs a variable voltage signal. Even assuming *arguendo* a skilled artisan would replace Nakai's resistor R8 with a transistor (as asserted by the Office Action), there is no suggestion that the skilled

[7] See Applicant's specification, page 12, lines 6-10; and page 12, line 22 – page 13, line 2.

artisan would also input a variable voltage signal to the control electrode of the substituted transistor.

There is no suggestion that the proposed modification of Nakai would produce a voltage at node W1 of Nakai (cited as teaching the claimed first bias voltage) which varies in accord with changes to the voltage at the gate of the substituted transistor (cited as teaching the claimed first transistor).

Accordingly, Applicant respectfully requests that the rejection of Claims 1 and 5 under 35 U.S.C. 103(a) as unpatentable over Nakai be withdrawn.

In addition to the above arguments in support of patentability, Applicant further notes Claim 3 recites that the first current generating part includes a current source; and includes "a second current mirror circuit ... generating a second mirror current of a similar value to that of said first minor circuit and letting said second mirror current flow to said first current electrode of said first transistor as said current".

The Office Action cites Narendra's resistor R1 of branch 102 as teaching the claimed current source; and cites Narendra's lower transistors (including the lower transistor of branch 102) as teaching the claimed second current mirror circuit.[8] Even though the current source and second current mirror circuit are part of the claimed bias voltage generating circuit, the Office Action also states that the claimed bias voltage generating circuit is read as ***only*** including branches 104, 106 (i.e., not including branch 102).[9] Clearly, these interpretations cannot establish Narendra as teaching the claimed elements in their claimed configuration.

Further, if the resistor R1 and lower transistors of branches 102, 106 are cited as teaching the claimed current source and second current mirror circuit (i.e., as part of the first claimed current generating circuit), then the portion of branch 102 extending from the resistor

[8] The "first current mirror circuit" of Claim 1 was previously recited as the "second current mirror circuit" of Claim 2.
[9] Office Action, 04/22/2005, page 3.

R1 to the lower transistor of branch 102 is being construed as teaching part of the bias generating circuit of Claim 1 (which includes the claimed first current generating part); and that portion of branch 102 cannot also be construed as carrying the claimed voltage signal input "from the exterior" of the bias voltage generating circuit of Claim 1.

Consequently, as all outstanding issues are believed to be addressed by the above remarks, Applicant submits that the present application is in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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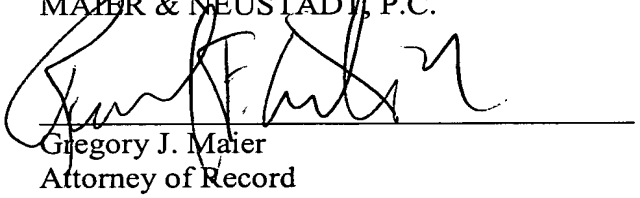

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